B4 amend

a conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region, wherein the conductive layer comprises a metal silicide.

REMARKS

At the outset, the undersigned expresses appreciation to the examiner for the thoroughness of the prior art search which formed the basis of the most recent office action. In particular, it is noted that the newly cited art does disclose functional features similar to the electrical functions achieved according to applicant's claims. Nonetheless, from a structural standpoint, the invention is quite distinguishable and the independent claims 1 and 15 have been amended to make these distinctions even more apparent.

Claims 1 – 31 are pending in the application. Claims 20 – 31 were withdrawn from consideration based on a restriction requirement made final. Applicant traversed the restriction requirement and again urges the examiner to reconsider the basis by which it was concluded that the claims of each group would result in a materially different product.

Claims 9 and 19 have been objected to as depending from rejected claims. All of the other claims were rejected under Section 102 based on Uenishi or Ishijima. Accordingly, the independent claims 1 and 15 are amended to more clearly distinguish the invention over the art of record. In addition, claims 9 and 19 are written in independent form. With these amendments, and in view of the remarks that follow, it is submitted that all of the claims are now in condition for allowance.

Applicants respectfully request the examiner to withdraw the rejections based on Uenishi and Ishijima because the independent claims now more expressly require

relationships not taught or suggested in any of the prior art. Specifically, with claim 1 now reciting "first and second spaced-apart doped regions extending into the surface from the plane ..." and with the claimed "third doped region ... positioned above the plane ..." it is more clearly apparent that the "conductive layer formed between the first and second regions and above the plane ..." is uniquely positioned. This structural configuration is not found in or suggested by the references.

Note, the rejection relied upon Ishijima for disclosing "a semiconductor layer 51 having a major surface formed along a plane 52" and "a third doped region, being the upper portion of part 53 ..." However, with the amendment to claim 1, the referenced portion of part 53 is not "above the plane ..." In applicant's claimed configuration Ishijima's "conductive layer 73" cannot be used to describe a structure that is "between the first and second regions and above the plane ..." See, for purposes of contrast, applicant's figure 6 which discloses an exemplary embodiment in which a conductive layer 120 does meet the terms of claim 1.

Claim 1 is also fully distinguished over Uenishi because applicant now requires the "third doped region ... positioned above the plane ..."

With regard to the rejection of claim 15 based on the Ishijima reference, claim 15 has also been amended to further distinguish the configuration. That is, the recited "conductor layer" is "in a plane extending between the first layer and the first field effect transistor channel region ..." See again Figure 6 for an example embodiment which meets these requirements.

For all of the above reasons, removal of the rejection is in order and it is respectfully submitted that the application is now in condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification, claims and abstract by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Respectfully,

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Version With Markings to Show Changes Made

(1) Kindly rewrite claim 1 as follows:

An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

first and second spaced-apart doped regions extending into [formed in] the surface from the plane;

a third doped region [over the first region] of different conductivity type than the first region, positioned above the plane and over the first region; and

a conductive layer formed between the first and second regions and above the plane, providing electrical connection between the doped regions.

(2) Kindly rewrite claim 9 as follows:

An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

first and second spaced-apart doped regions formed in the surface;

a third doped region over the first region of different conductivity type than the first region; and

a conductive layer formed between the first and second regions and above the plane, providing electrical connection between the doped regions, [The structure of claim 1] wherein the conductive layer comprises one or more materials taken from the group comprising tungsten silicide, tungsten nitride, titanium silicide, titanium nitride and cobalt silicide.

(3) Kindly rewrite claim 15 as follows:

A semiconductor device comprising:

a first layer of semiconductor material;

a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region;

a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and

a conductive layer in a plane extending between the first layer and the first field effect transistor channel region, said conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

(4) Kindly rewrite claim 19 as follows:

A semiconductor device comprising:

a first layer of semiconductor material;

a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region;

a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and

a conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region, [The device of claim 15] wherein the conductive layer comprises a metal silicide.